

SOC Implementation & Physical Design

Director, Core Engineering (China)

Primary Objectives:

The position is responsible for supporting, managing and directing a team of Digital designers in China core engineering business unit of Conexant Systems Inc. Major responsibilities include complete ownership of ASIC implementation activities, supporting the RTL to GDSII SoC ASIC flow, managing and expanding the engineering team. The candidate should be able to direct 2 to 3 teams in support of complex SoC implementations concurrently.

Specific Responsibilities:

The management of the engineering team, responsible for the development and support of current and future products development, includes:

- Working with US teams to adopt the Conexant SoC design flow.
- Must be able to communicate and drive the cross functional teams located in worldwide locations.
- Recruiting, managing, and training the team of about 20 engineers initially.
- Planning and managing all projects to be predictable, on time and on budget.
- Planning the capital and labor budgets required to support the engineering activities including new programs.
- Implementing good design practices and other methodologies.
- Working with US based teams to improve design methodology adoption.

Position Requirements:

Required Attributes: This is a highly technical position, and the successful candidate must be able to quickly command respect from a team of senior engineers for his/her engineering knowledge, judgment, and experience. The successful candidate will be measured on his/her ability to plan a complex workload in a rapidly changing environment, deliver high quality products on time and within budget, and maximize the productivity of the design team. Specific required and desired attributes include:

- BSEE degree required, MSEE EE preferred.
- 10+ years of hands-on experience in IC implementation with several tapeouts, preferably in advanced processes like 90nm and 65nm.
- Experience with industry tools like Magma & Synopsys
- Well versed in Synthesis, Timing Closure, Formal verification and Backend related issues.

- Must be able to handle and drive the project from start to finish including chip partitioning, establishing and implementing power saving techniques.
- Leader with outstanding technical and analytical skills and commitment to success.
- Proven ability to manage product development activity (from inception to production release) per an aggressive schedule; able to make trade-offs that optimize around a project's primary goals with disciplined approach.
- Experience with Foundation IP like standard cells memory compilers a plus
- Experience working closely with product management
- Extremely driven individual that is able to successfully set priorities, drive decisions and get closure on recommendations and issues.
- Excellent interpersonal, organizational, and leadership skills.
- Excellent scheduling, budgeting, resource loading, and overall planning skills.
- Strong verbal and written communication skills.
- Self-motivated and able to work well autonomously.