

Job Description

Sr. Communication Systems Engineer/Manager

Responsible for RF system architecture development, evaluation and lab testing for wireless communication system, and lead in baseband system architecture, integration with RF system, and evaluation of the complete communication system. Requires 5+ years hand-on experience on communication system design and RF system architecture design. Requires solid understanding of the fundamentals of signal processing and communication theories, and strong analytical skills; good verbal and written communication skills; and ability to work independently and lead the system technical work. Experience in multi-carrier communications, timing/carrier recovery, convolutional codes, Reed-Solomon codes, LDPC codes, channel estimation and equalization, wireless channel modeling is a plus.

Sr. RFIC design Engineer 1/Manager

Responsible for the IC design of various broadband RF front end blocks with good understanding of trade offs between different circuit topologies. Design responsibility includes both low-level circuit design as well as top-level functionality and performance simulation and lab verification. Requires MSEE with at least 5 years of experience designing relevant RFIC circuits. Extensive experience with designing and measuring RF front-end blocks, i.e. LNA, Mixer, RF VGA, RF variable attenuator. Good simulation methodology for both the low and top-level blocks is required. In depth knowledge of parasitic extraction both at the die level as well as package and PCB level is required. Good team oriented design approach and collaboration experience with RF system, test and product engineering. Basic Analog IC design experience as well as RF IC design experience is required. In depth experience with Cadence and/or ADS and basic knowledge of Virtuoso layout CAD tools are required. RFIC design and device modeling experience outside the RF blocks is a plus.

Sr. RFIC design Engineer 2/Manager

Responsible for the IC design of broadband synthesizer and other key RF blocks. Design responsibility includes both low-level circuit design as well as top-level functionality and performance simulation and lab verification. Requires MSEE with at least 5 years of experience designing relevant RFIC circuits. Extensive experience with designing and measuring RF synthesizer and clock management circuits, which include PLL, VCO, high-frequency divider and prescaler, digital counter, phase/frequency detector, charge pump, PLL loop filter, crystal oscillator, and etc. Good simulation methodology for both the low and top-level blocks is required. Good team oriented design approach and collaboration experience with RF system, test and product engineering. Basic Analog IC design experience as well as RF IC design experience is required. In depth experience with Cadence and/or ADS and basic knowledge of Virtuoso layout CAD tools are required. Analog IC design experience outside the RF blocks or DSP background is a plus.

Sr. Analog IC design Engineer /Manager

Responsible for the IC design of analog filters, variable gain amplifiers and other analog blocks for RF communication system with good understanding of trade offs between different circuit topologies. Design responsibility includes both low-level circuit design as well as top-level functionality and performance simulation and lab verification. Requires MSEE with at least 5 years of experience designing relevant analog circuits. Extensive experience with designing and measuring analog blocks for RF communication system, i.e. analog filter, variable gain amplifiers, DC offset cancellation, process and temperature calibration, bandgap, and etc. Good simulation methodology for both the low and top-level blocks is required. In depth knowledge of parasitic extraction is required. Good team oriented design approach and collaboration experience with RF/analog system, test and product engineering. In depth experience with Cadence and basic knowledge of Virtuoso layout CAD tools are required. ESD design and power management design experience is a plus.

Sr. Mixed-signal design Engineer/Manager

Responsible for the mixed-signal architecture and IC design of wide-band/high data rate ADC/DAC, filters, and other mixed-signal blocks for communication system, with good understanding of trade offs between different circuit topologies. Design responsibility includes both low-level circuit design as well as top-level functionality and performance simulation and lab verification. Requires MSEE with at least 5 years of experience designing relevant circuits and solid understanding of signal processing. Extensive experience with designing and measuring mixed-signal blocks for communication system, i.e. ADC, DAC, filter, process and temperature calibration, etc. Good simulation methodology for both the low and top-level blocks is required. In depth knowledge of parasitic extraction is required. Good team oriented design approach and collaboration experience with RF/analog system, test and product engineering. In depth experience with Cadence and basic knowledge of Virtuoso layout CAD tools are required.