Cypress solutions are at the heart of any system that is built to *perform*: consumer, computation, data communications, automotive, industrial, and solar power. Leveraging a strong commitment to customer service and performance-based process and manufacturing expertise, Cypress's product portfolio includes a broad selection of wired and wireless USB devices, CMOS image sensors, timing solutions, network search engines, specialty memories, high-bandwidth synchronous and micropower memory products, optical solutions, and reconfigurable mixed-signal arrays. Cypress stock is traded on the New York Stock Exchange under the ticker symbol CY.

The following positions are open in Shanghai, China. Please send all resumes of interested candidates to **LBN@cypress.com** with the job title in the subject line.

CYPRESS CHINA FINANCE DIRECTOR

Responsibilities:
Provide Finance support for all Cypress operations in China (Asia-Pac Sales, Manufacturing, IP licensing, Design, and Support groups). Business partner for Cypress China management. Contract negotiations/reviews for foundries, subcontractors and customers. Coordinate banking, tax and legal issues. Develop inputs on Cypress Semiconductor sales and expenses in China for quarterly and annual plans. Provide analytical support for Cypress China management. Coordinate monthly close activities for China operations with the International Finance group. Finance owner for Cypress China P&L. Ensure compliance with U.S. reporting and Sarbanes-Oxley requirements. Office management for Cypress Shanghai groups.

Requirements:
BS or BA Degree in Finance or Accounting. MBA and/or CPA preferred. At least ten years accounting/finance experience. High tech/semiconductor experience is also preferred.

SENIOR ASIC VERIFICATION ENGINEER

Responsibilities:
Will be a core member of a custom mixed-signal IC design team. Primary responsibility will be to test bench development and verification test of custom IC logic designs, working with others involved in verification and test development. Must be able to effectively reduce system and IC module specifications into written verification requirements (development of verification plans, detailed specifications, test bench functional requirements, test vectors, etc.) Design of Vera and Verilog test benches for efficient and flexible use by self and others. Verification of custom IC logic designs and reporting of functional simulation and code coverage results. Assist logic/circuit designers with debug efforts to achieve full functionality and code coverage metrics of IC designs. Document test bench designs and participate in design reviews in accordance with department development process and company quality standards. Test bench support, maintenance and user training. Ability to develop and conduct testing of physical silicon using logic analyzers, oscilloscopes, and other common laboratory equipment is a plus. Ability to port synthesizeable RTL logic designs into FPGA implementations for rapid prototyping is a plus.

Requirements:
Able to communicate in English effectively, team player who is able to take initiatives and set high goals, smart and confident, self starter & ability to work in a team environment as an individual contributor, and also possess a track record of planning and delivering work completely and on time. 5 years Verilog test bench development & behavioral verification of custom IC designs experience needed as well as 3-5 years synthesizable Verilog logic design for custom ICs experience. Expert in Vera code development. Proficiency in Perl, Tcl, Tk, C++, and C# languages. Master's Degree or above in EE/CE.

ASIC LOGIC/CIRCUIT DESIGN ENGINEER

Responsibilities:
As a logic designer, will be responsible for writing HDL code, synthesis, logic verification, and static timing analysis for pre and post layout. Must have experience with Verilog and/or VHDL and Synopsys Design Compiler and PrimeTime. Knowledge of place and route strongly encouraged. As a circuit designer, must be familiar with Cadence's Composer for schematic entry, transistor-level circuit simulation tools. Must be familiar with Calibre DRC/LVS tools.

Requirements:
Able to communicate in English effectively, team player who is able to take initiatives and set high goals, smart and confident, self starter & ability to work in a team environment as an individual contributor, and also possess a track record of planning and delivering work completely and on time. 3-5 years as ASIC/circuit design engineer. Strong knowledge of CMOS device and circuit fundamentals. Master's Degree or above in EE/CE.

AE MANAGER, SHANGHAI PSOC SOLUTIONS CENTER

Responsibilities:
Manage award-winning PSoC programmable mixed-signal array microcontroller Solutions Center. Provide reference/demo design in embedded control applications. Key customer and distributor technical support. Develop and deliver presentations to customers. Work with marketing to exchange technical input on marketing collateral, new product definition, product features prioritization, customer feedback, and product training curriculum. Work with design engineering to exchange technical support/sustaining engineering support, new product development interactions, impact of design limitations.

Requirements:
Strong embedded microcontroller background. Fluent in Mandarin and able to communicate effectively in English. Hard working and team player. Takes initiative and sets high goals. Customer service orientation. Smart and confident. Minimum of five+ years in engineering management position. Master's Degree or above in EE/CE.

HARDWARE APPLICATION ENGINEER - SHANGHAI PSOC SOLUTIONS CENTER

Responsibilities:
Develop hardware/board designs for award-winning PSoC programmable mixed-signal array microcontroller. Provide reference design in embedded control applications. Key customer and distributor technical support. Develop and deliver presentations to customers. Work with marketing to exchange technical input on marketing collateral, new product definition, product features prioritization, customer feedback, and product training curriculum. Work with design engineering to exchange technical support/sustaining engineering support, new product development interactions, impact of design limitations

Requirements:
Capable of creating schematics, BOM, and board layout. Competent at board bring-up, debug. Fluent in English (both written and oral). Hard working and team player. Takes initiative and sets high goals. Customer service orientation. Smart and confident. Minimum of five years in semiconductor applications or system design. 4+ years PCB expertise. Bachelor's Degree (4 year college) or above in EE/CE.

FIRMWARE APPLICATION ENGINEER – SHANGHAI PSOC SOLUTIONS CENTER

Responsibilities:
Develop firmware for award-winning PSoC programmable mixed-signal array microcontroller. Provide reference design in embedded control applications. Key customer and distributor technical support. Develop and deliver presentations to customers. Work with marketing to exchange technical input on marketing collateral, new product definition, product features prioritization, customer feedback, and product training curriculum. Work with design engineering to exchange technical support/sustaining engineering support, new product development interactions, impact of design limitations

Requirements:
Solid "C" code familiarity (code generation, compiling, debugging). Knowledgeable on analog and MCU design. Fluent in English (both written and oral). Hard working and team player. Takes initiative and sets high goals. Customer service orientation. Minimum of five years in semiconductor applications or system design. 2yrs+ embedded microcontroller (8-bit, 16bit)/embedded control application background. Bachelor's Degree (4 year college) or above in EE/CE.

PROCESS DEVICE ENGINEER PRIINCIPAL

Responsibilities:
In charge of transfer of deep submicron photolithography processes from Cypress Semiconductor manufacturing and R&D fabs in U.S. and their qualification in CY foundry partner in Shanghai, China. Will collaborate with CY R&D and manufacturing process and integration engineers and foundry partner's process and integration engineers to find and fix root cause for photolithography related yield limiting failure modes. Will collaborate with CY and foundry partner design and CAD groups in defining the requirements for various product tape out. Will employ advanced DOE and statistical analysis software and state-of-the-art analytical equipments and techniques to obtain fundamental understanding and practical solutions to complex photolithography related challenges.

Requirements:

Experience with submicron photolithography tracks, scanners, and illumination methods. Knowledge of photo resist and antireflective coating materials. Familiar with DOE techniques and SPC applications. Familiar with high volume submicron manufacturing environment, team player with good interpersonal and communication skills. Strong command of written and spoken English language is highly desired. Ph.D degree or MS degree in EE, Material Science, Chem. E or Physics with 1 to 3+ years experience in photolithography process development.

PROCESS DEVICE ENGINEER SENIOR STAFF

Responsibilities:
PHOTOLITHOGRAPHY: In charge of transfer of deep submicron photolithography processes from Cypress Semiconductor manufacturing and R&D fabs in U.S. and their qualification in CY foundry partner in Shanghai, China. Will collaborate with CY R&D and manufacturing process and integration engineers and foundry partner's process and integration engineers to find and fix root cause for photolithography related yield limiting failure modes. Will collaborate with CY and foundry partner design and CAD groups in defining the requirement for various product tape out. Will employ advanced DOE and statistical analysis software and state-of-the-art analytical equipments and techniques to obtain fundamental understanding and practical solutions to complex photolithography related challenges.

Requirements:
PhD degree or MS degree in EE, Material Science, Chem. E or Physics with 1 to 3+ years experience in photolithography process development. Experience with submicron photolithography tracks, scanners and illumination methods. Knowledge of photo resist and antireflective coating materials. Familiar with DOE techniques and SPC applications. Familiar with high volume submicron manufacturing environment. Team player with good interpersonal and communication skills. Strong command of written and spoken English language is highly desired. PhD degree or MS degree in EE, Material Science, Chem. E or Physics with 1 to 3+ years experience in photolithography process development.

SENIOR TECHNOLOGY DEVELOPMENT ENGINEER

Responsibilities:
In charge of coordination of module activities, design of experiments and split lots, analysis of electrical and reliability data during technology transfer from Cypress Semiconductor manufacturing fabs in U.S. and qualification in CY foundry partners. In charge of driving failure mode analysis and yield enhancement through working with CY manufacturing and R&D process development engineers and foundry partners process development and integration engineers.

Requirements:
Experience with split lot design and electrical data analysis software and techniques. Sound knowledge of IC submicron IC manufacturing processes. Familiar with design of experiment (DOE) and SPC. Team player with leadership skills and excellent interpersonal and communication skills. Strong knowledge of CMOS and analog device characterization and theory is highly desired. Strong command of written and spoken English language is highly preferred. Ph.D or MS degree in EE or Physics with 2 to 4+ years experience in technology integration.

TECHNOLOGY DEVICE ENGINEER STAFF

Responsibilities:
In charge of device characterization for new technologies transferred to CY foundry partners. Work with CY and founry partners integration engineers and product engineers to properly characterize various analog and digital devices and enable successful device qualification and yield enhancement.

Requirements:
Strong knowledge of device characterizations for analog and/or nonvolatile devices is highly preferred. Good interpersonal and communication skills. Good command of written and spoken English language is highly preferred. Ph.D degree or MS degree in EE, Material Science Chem. E or Physics with 1 to 3+ years experience as a Yield Engineer.